UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,180	10/23/2001	Jerome Tjia	SG 010008	9013

24738 7590 10/21/2005

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,180	TJIA, JEROME	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larky et al. (US Patent 6,311,294) in view of Watson et al. (US Patent 6,218,969)

As per claim 1, Larky discloses a bus system(fig.4, 42) comprising a first (fig.4, 12) and second (fig.4, 14) station coupled via a bus for transferring data and control signals, the bus operating according to a protocol in which the first station repeatedly sends requests for data to the second station, the second station responding to each request by sending a message with a data item or sending a negative acknowledge signal, wherein the second station comprises: (col.2, lines 36-48), (col.3, lines 18-38)

- an interruptable processor (fig.4, 56) for generating data items; (col.2, lines 36-48, wherein simultaneously requesting implies interruptable)
- a first in first out buffer coupled between the processor and the bus, for buffering data items for successive messages in a first in first out order, the processor being programmed to start writing the data items to the buffer in response to an interrupt. (col.4, lines 26-67, wherein logical data pipe 34 implies FIFO)

- a bus interface arranged to handle the protocol, sending data items from the buffer in the messages,

Larky discloses all the limitations as above except the bus interface sending an interrupt to the processor in response to selected ones of the requests, when the buffer is empty and no interrupts have yet been generated since the processor has written into the buffer. However, Watson discloses identified an interrupt request whether data is available. If data available the data is sent through the usb device controller to the host and then awaits for an acknowledgement of receipt of the transferred data. If the data transfer is acknowledge, the universal device controller interface then signals that a valid transfer. If determined the requested data is not available then a not acknowledge signal is sent to usb bus. In addition, Watson discloses the decision is made as to whether there is sufficient storage space in the buffer to received the data. (col.7, lines 7-62)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Watson's teaching into Larky's system so as to provide a signal converter which can operate in a register mode wherein the signal converter contains a set of registers which emulate those found in standard computer parallel port hardware. (col.2, lines 34-39)

As per claims 2,9, Larky discloses wherein the bus system is a USB bys system. (fig.4, 42)

As per claims 3, 5, Larky discloses wherein the bus interface is arranged generate an interrupt signal in response to an acknowledge signal from the first station after sending the message. (col.6,lines 13-58)

As per claims 4 and 8, Larky discloses a bus interface integrated circuit, comprising:

- a connection for a bus; (fgi.2, col.4, lines 26-38)
- a first in first out buffer; (fig.3, 32, col.4,lines 26-38)
- an interrupt output for applying an interrupt to a processor; (col.7, lines 18-29)

Larky discloses all the limitations as above except a controller arranged to receive requests for data from the connection, and to respond to the requests by sending a message containing a data item from the buffer if the buffer is not empty, or by sending a negative acknowledge signal to the connection if the buffer is empty and to send an interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer. However, Watson discloses identified an interrupt request whether data is available. If data available the data is sent through the usb device controller to the host and then awaits for an acknowledgement of receipt of the transferred data. If the data transfer is acknowledge, the universal device controller interface then signals that a valid transfer. If determined the requested data is not available then a not acknowledge signal is sent to usb bus. In addition, Watson discloses the decision

is made as to whether there is sufficient storage space in the buffer to received the data. (col.7, lines 7-62)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Watson's teaching into Larky's system so as to provide a signal converter which can operate in a register mode wherein the signal converter contains a set of registers which emulate those found in standard computer parallel port hardware. (col.2, lines 34-39)

As per claim 6, Larky discloses an integrated circuit arranged to be switchable between a plurality modes of operation, (col.4, lines 26-67, wherein different type of data implies modes of operation)

Larky discloses all the limitations as above except the integrated circuit generating the interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer in a first one of the modes, the integrated circuit generating an interrupt signal in response to an acknowledge signal from the bus after sending the message in a second one of the modes. However, Watson discloses identified an interrupt request whether data is available. If data available the data is sent through the usb device controller to the host and then awaits for an acknowledgement of receipt of the transferred data. If the data transfer is acknowledge, the universal device controller interface then signals that a valid transfer. If determined the requested data is not available then a not

acknowledge signal is sent to usb bus. In addition, Watson discloses the decision is made as to whether there is sufficient storage space in the buffer to received the data. (col.7, lines 7-62)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Watson's teaching into Larky's system so as to provide a signal converter which can operate in a register mode wherein the signal converter contains a set of registers which emulate those found in standard computer parallel port hardware. (col.2, lines 34-39)

As per claim 7, Larky discloses an integrated circuit arranged to be switchable between a plurality modes of operation, (col.4, lines 26-67, wherein different type of data implies modes of operation)

Larky discloses all the limitations as above except the integrated circuit generating said interrupt signal in response to each request for data when the buffer is empty in a first one of the modes, the integrated circuit generating the interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer in a second one of the modes. However, Watson discloses identified an interrupt request whether data is available. If data available the data is sent through the usb device controller to the host and then awaits for an acknowledgement of receipt of the transferred data. If the data transfer is acknowledge, the universal device controller interface then signals that a valid

transfer. If determined the requested data is not available then a not acknowledge signal is sent to usb bus. In addition, Watson discloses the decision is made as to whether there is sufficient storage space in the buffer to received the data. (col.7, lines 7-62)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Watson's teaching into Larky's system so as to provide a signal converter which can operate in a register mode wherein the signal converter contains a set of registers which emulate those found in standard computer parallel port hardware. (col.2, lines 34-39)

Response to Amendment

3. Applicant's amendment filed on 7/25/05 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

October 17, 2005

Primary Examiner